Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A random number generator comprising:

a plurality of groups of independent flip-flops ~~each~~, at least some of the groups having different ~~configurations; and~~ connection configurations,

an exclusive-or (XOR) network connected to all ~~each~~ of the outputs of the plurality of groups of flip-flops ~~being connected in an exclusive-or (XOR) network, a latch connected to the output of the XOR network~~, wherein a metastable output of at least one ~~of~~ flip-flop of the plurality of groups of flip-flops causes a random signal to be output by the XOR network for number generation, and

a latch connected to the output of the XOR network.

2. (original) The random number generator according to claim 1, wherein the groups of flip-flops are divided into at least three equally-sized groups.

3. (currently amended) The random number generator according to ~~claim 2,~~ claim 1, wherein ~~the~~ a first group of flip-flops comprises ~~pairs~~ a first pair of cross-connected NAND gates without any buffers ~~inserted between the~~ connected to first data and clock ~~signals~~ input lines,

wherein ~~the~~ a second group of flip-flops comprises ~~at least one~~ a second pair of cross-connected NAND gates with a first buffer connected to a second data input line of at least one NAND gate of the ~~at least one~~ second pair of NAND gates ~~being connected via a buffer~~; and

wherein ~~the~~ a third group of flip-flops comprises ~~at least one~~ a third pair of cross-connected NAND gates ~~having~~ with a second buffer connected to a second clock input

line of at least one NAND gate of ~~each of~~ the ~~pairs~~ third pair of NAND gates ~~being connected via a buffer~~.

4. (currently amended) The random number generator according to ~~claim 2,~~ claim 1, wherein a first group of flip-flops comprises ~~at least~~ a first pair of cross-connected NAND gates without any buffers ~~between the~~ connected within a cross connection between the first pair of NAND gates, and

wherein ~~the~~ a second group of flip-flops comprises ~~at least one~~ a second pair of cross-connected NAND gates ~~having~~ with a delay buffer connected within a cross connection between ~~to the output of an upper NAND gate of~~ the NAND gates of the second pair of the NAND gates, ~~and~~

~~wherein the third group of flip-flops (334) comprises at least one pair of cross-connected NAND gates having a delay buffer connected to the output of a lower NAND gate of each pair of the NAND gates~~.

5. (currently amended) The random number generator according to ~~claim 2,~~ claim 1, wherein ~~the~~ a first group of ~~flip-flops (394)~~ flip-flops comprises ~~at least one~~ a first pair of cross-connected NAND gates without any load ~~added~~ connected to either of the NAND gates,

wherein ~~the~~ a second group of ~~flip-flops~~ flip-flops comprises ~~at least one~~ a second pair of cross-connected NAND gates ~~having~~ with a first capacitive load connected to ~~the~~ a data input line of at least one NAND gate of the second pair of NAND gates, and

wherein ~~the~~ a third group of ~~flip-flops~~ flip-flops comprises ~~at least one pair~~ a third pair of cross-connected NAND gates ~~having~~ with a second capacitive load connected to ~~the~~ a clock input of at least one NAND gate of ~~each of~~ the ~~at least one~~ third pair of NAND ~~gates~~ gates.

6. (currently amended) The random number generator according to claim 5, ~~wherein the capacitive load~~ wherein at least one capacitive load of the first and second capacitive loads comprises a ~~multi-input~~ multi-input gate.

7. (currently amended) The random number ~~generator~~ generator according to claim 1, wherein the groups of ~~flip-flops have~~ flip-flops comprise unequal numbers of flip-flops ~~flip-flops~~ in each group.

8. (currently amended) The random number generator according to claim 1, wherein delay devices connected within each of the groups of flip-flops ~~flip-flops~~ have different delay values.

9. (currently amended) The random number generator according to claim 1, wherein ~~a portion of the flip-flops are NAND gates, and the remainder are~~ at least some of the NAND gates are implemented with Boolean equivalents of NAND gates.

10. (currently amended) The random number generator according to claim 1, wherein the groups of ~~flip-flops~~ flip-flops are arranged into one of thirds or fifths.

11. (currently amended) A method for random number generation, comprising ~~the steps of~~

~~(a)~~ providing a plurality of groups of independent ~~flip-flops, each~~ flip-flops, at least some of the groups having different ~~configurations; and~~ connection configurations,

~~(b)~~ connecting each of the outputs of the plurality of groups of ~~flip-flops in~~ flip-flops to an exclusive-or (XOR) network, ~~(c) connecting a latch at the output of the XOR, so that~~ wherein a metastable output of at least one of ~~flip-flops cause~~ flip-flops causes a random signal to be output by the XOR network ~~for receiopt by the latch for random number generation~~, and

connecting a latch to the output of the XOR network to receive the random signal output by the XOR network for random number generation.

12. (currently amended) The method according to claim 11, wherein ~~step (a)~~ providing the plurality of independent flip-flops further comprises:

~~(i)~~ arranging the groups of flip-flops into three equally-sized groups.

13. (currently amended) The method according to ~~claim 12,~~ claim 11, wherein a first group comprises ~~at least one~~ a first pair of cross-connected NAND ~~gates~~ gates without any buffers ~~inserted between the~~ connected to first data and clock ~~signals~~ input lines,

wherein ~~the~~ a second group comprises ~~at least one~~ a second pair of cross-connected NAND gates with a first buffer connected to a second data input line of at least one NAND gate of ~~each of~~ the second pair ~~pairs~~ of NAND gates ~~being connected via a buffer~~; and

wherein ~~the third group~~ a third group comprises ~~at least one~~ a third pair of cross-connected NAND gates ~~having~~ with a second buffer connected to a second clock input line of at least one NAND gate of ~~each of~~ the third ~~pairs~~ pair of NAND gates ~~being connected via a buffer~~.

14. (currently amended) The method according to ~~claim 12,~~ claim 11, wherein a first group comprises ~~at least one~~ a first pair of cross-connected NAND gates without any buffers ~~between the~~ connected within a cross connection between the first pair of NAND gates, and

~~the~~ wherein a second group comprises ~~at least one~~ a second pair of cross-connected NAND gates ~~having~~ with a delay buffer connected within a cross connection between ~~to the output of an upper NAND gate of each pair of~~ the NAND gates of the second pair of NAND gates, ~~and~~

~~the third group comprises at least one pair of cross-connected NAND gates having a delay buffer connected to the output of a lower NAND gate of each pair of the NAND gates~~.

15. (currently amended) The method according to ~~claim 12,~~ claim 11, wherein a first group comprises ~~at least one~~ a first pair of cross-connected NAND gates without any load ~~added~~ connected to either of the NAND gates,

wherein ~~the~~ a second group comprises ~~at least one~~ a second pair of cross-connected NAND gates ~~having~~ with a first capacitive load connected to ~~the~~ a data input line of at least one NAND gate of ~~each of the pairs~~ the second pair of NAND gates, and

wherein ~~the~~ a third group comprises ~~at least one~~ a third pair of cross-connected NAND gates ~~having with~~ a second capacitive load connected to ~~the~~ a clock input line of at least one NAND gate of ~~each of~~ the ~~pairs~~ third pair of NAND gates.

16. (currently amended) The method according to claim 15, wherein at least one capacitive load of the first and second capacitive ~~load provided~~ loads comprises a multi-input gate.

17. (currently amended) The method according to claim 11, wherein ~~step (a)~~ providing the plurality of groups of independent flip-flops further ~~includes (i)~~ comprises arranging the groups of ~~flip-flops~~ flip-flops ~~so that there are~~ to define groups with unequal numbers of ~~flip-flops~~ flip-flops in each group.

18. (currently amended) The method according to claim 11, wherein each of the ~~groups~~ groups of flip-flops have different delay values.

19. (currently amended) The method according to claim 11, wherein providing ~~a portion of~~ the plurality of groups of independent flip-flops ~~provided in step (a) are~~ comprises providing NAND ~~gates,~~ gates and ~~the remainder are~~ Boolean equivalents of NAND gates.

20. (currently amended) The method according to claim 11, wherein the groups of ~~flip-flops~~ flip-flops are arranged into one of thirds or fifths.